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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,780	07/21/2003	Atsushi Yusa	OKI.553	4253

20987 7590 10/16/2006

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EXAMINER	
LE, DIEU-MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,780	YUSA, ATSUSHI	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed 08/03/2006 in application 10/622,780.

2. Claims 1-18 are again presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuda et al. (U.S. Patent No. 5,132,937 hereafter referred to as Tuda) in view of Kono et al. (U.S. Patent 5,455,536 hereafter referred to as Kono).

As per claim 1:

Tuda explicitly teach the invention. Tuda teaches:

- A circuit for detecting an abnormal operation of memory [abstract, col. 2, lines 44-60] comprising:
- a delay circuit for delaying an output data output from the memory for a predetermined period of time and for outputting a delayed data responsive thereto [col. 4, lines 2-41 and col. 6, lines 31-58];

Tuda does not explicitly teach:
- a comparison circuit for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other.

However, Tuda does disclose capability of:
- a semiconductor memory testing including a delay circuit, a comparison circuit, and input/output data [abstract, fig. 3A and 6, col. 2, lines 44-60] comprising capabilities of:
- ***comparing/detecting circuit used for comparing outputs from data sub-array via multiplexer and amplifier [col. 4, lines 2-41 and col. 6, lines 38-58***].

In addition, Kono does explicitly disclose:
- An error detection and correction system having BER monitor [abstract, col. 1, lines 1-12] comprising
- ***a comparison circuit for outputting a not coincident signal from carrying out a comprison between the data and delayed data*** [col. 2, lines 29-50].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to first realize that the combination of Tuda's ***signal resetting***

and execution in the semiconductor memory capability and Kono's ***comparison circuit for outputting a not coincident signal from carrying out a comprison between the data and delayed data*** do perform such Applicant's comparison circuit for outputting a noncoincidence signal limitation. This is because Tuda and Kono clearly applied these circuitries for testing configuration, comparison, simulation, evaluation, performance in determining whether the system functioned properly; second, by applying the combined ***delayed and comparison capabilities in supporting the failure detection process*** as taught by Kono in conjunction with the ***comparing/detecting circuit used for comparing outputs from data sub-array via multiplexer and amplifier*** as taught by Tuda, the computer memory data processing system, more specifically an memory abnormal operation detection system can enhance its operation performance, more specifically to ensuring the error thoroughly detected and corrected via the delaying and comparison processes.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer memory data system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data displaying, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 2-4:

Tuda further explicitly teach:

- an access speed of the memory is detected (i.e., ***read/write and storing to and from memory***) [col. 4, line 45 through col. 5, line 25];
- a circuit for holding address information in case of noncoincidence in response to the noncoincidence signal [col. 4, lines 2-41];
- a circuit for sounding an alarm when the noncoincidence signal is output (i.e., ***indicating signal***) [col. 1, lines 57-67].

In addition, Kono does explicitly disclose:
- An error detection and correction system having BER monitor [abstract, col. 1, lines 1-12] comprising
- ***an error indication pulse used when data are not coincident*** [col. 2, lines 51-64].

As per claim 6:

Tuda further explicitly teach:
- a delay time of the output data of the memory can be adjusted in the delay circuit [col. 4, lines 2-41 and col. 5, line 67 through col. 6, line 3].

As per claims 8 and 18:

Due to the similarity of claims 8 and 18 to claims 1-4 except for an integrated circuit comprising a memory, delaying circuit, and comparison circuit etc… instead of a circuit for detecting an abnormal operation of memory comprising capabilities of a memory, delaying circuit, comparison circuit, etc…; therefore, this claim is also rejected under the same rationale applied against claims 1-4. **In addition, all of the**

limitations have been noted in the rejection as per claims 1-4 (i.e., an integrated circuit comprising a circuit for detecting an abnormal operation of memory (i.e., ***semiconductor memory device***) [abstract, col. 2, lines 44-60]).

As per claims 9-12, 14-15:

Due to the similarity of claims 9-12, 14-15 to claims 1-4 and 6 except for a method for detecting an abnormal operation of memory comprising delaying and output step, outputting an incoincidence signal step, comparison step, etc… instead of a circuit for detecting an abnormal operation of memory comprising capabilities of delaying, output, outputting an incoincidence signal, comparison, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-4 and 6 . **In addition, all of the limitations have been noted in the rejection as per claims** 1-4 and 6.

As per claims 5, 7, 13, and 16:

Tuda explicitly teach the invention. Tuda teaches:

- A circuit for detecting an abnormal operation of memory [abstract, col. 2, lines 44-60] comprising:
- a delay circuit for delaying an output data of the memory for a predetermined period of time and for outputting this data as a delay data [col. 4, lines 2-41].

Tuda does not explicitly teach:

- a circuit for executing an interruption;
- a flash memory.

However, Tuda does disclose capability of:

- a semiconductor memory testing including a delay circuit, a comparison circuit, and input/output data [abstract, col. 2, lines 44-60] comprising capabilities of:

- ***signal resetting and executing in supporting the memory failure detecting [col. 4, lines 20-41 and col. 5, lines 57-66]***.

- a semiconductor memory (i.e., ***flash memory***) [col. 1, lines 8-11].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that the Tuda's ***signal resetting and execution in the semiconductor memory*** capability does perform such Applicant's interrupting and flash memory limitations. This is because Tuda clearly applied these features therein for testing configuration, comparison, simulation, evaluation, performance in determining whether the memory system functioned properly. It is further obvious because these interrupting and flash memory features are notoriously well-known in the art of memory testing and failure/abnormal detection and correction arena. By applying the Tuda's ***signal resetting and execution in the semiconductor memory*** capability, the computer memory data processing system, more specifically an memory abnormal operation detection system can enhance its operation performance, more specifically to ensuring the error thoroughly detected and corrected via the delaying and comparison processes.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer memory data system operation

availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data displaying, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claim 17:

Tuda further teaches:

- a delay circuit for delaying an output data of the memory for a predetermined period of time and for outputting this data as a delay data [col. 4, lines 2-41].

Tuda does not explicitly teach:

- a first and second latches circuits for stores output data and the delayed data.

However, Tuda does disclose capability of:

- ***operation of result storing mode used in supporting error detection and correction*** [col. 5, lines 8-25].
- a semiconductor memory (i.e., ***flash memory***) [col. 1, lines 8-11].

In addition, Kono does explicitly disclose:

- An error detection and correction system having BER monitor [abstract, col. 1, lines 1-12] comprising
- ***latch circuit used in supporting error detection/correctin and data comparison process*** [col. 2, lines 29-50].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to first realize that the combination of Tuda's ***operation of result storing mode used in supporting error detection and correction*** capability and Kono's ***latch circuit used in supporting error detection/correctin and data comparison process*** do perform such Applicant's first and second latches circuits for stores output data and the delayed data limitation. This is because Tuda and Kono clearly applied these circuitries for testing configuration, comparison, storing, simulation, evaluation, performance in determining whether the system functioned properly; second, by utilizing this approach, the computer memory data processing system can enhance its operation performance for the same reasons set forth as described in claim 1, **supra.**

Applicant's arguments with respect to claims -18 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action

is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday
from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman, can be reached on (571)272-3644.
The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

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05/09/06